METHOD, CIRCUIT LIBRARY AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING ENHANCED PERFORMANCE AND REDUCED LEAKAGE CURRENT FOR ASIC DESIGNS

Field of the Invention

5   The present invention relates generally to the data processing field, and more particularly, relates to a method, circuit library and computer program product for implementing application specific integrated circuit (ASIC) designs having enhanced high performance and reduced leakage current.

10   **Description of the Related Art**

The current trend in CMOS integrated circuit library design is to offer multiple threshold voltage (VT) variations of the circuit library. Known circuit libraries include circuits formed of standard VT (SVT) devices, or circuits formed of low VT (LVT) devices. Typically, SVT devices are used in a

15   normal circuit design.

FIG. 1A shows a schematic of an SVT inverter circuit in a Standard Cell Library, and FIG. 1B shows the corresponding SVT layout.

FIG. 2A shows a schematic of an LVT inverter circuit in a Standard Cell Library, and FIG. 2B is the corresponding LVT layout. For high

20   performance, circuits comprised of 100% LVT devices can be substituted for their normal and longer delay SVT counterparts. A disadvantage of this

approach is that the leakage current of the LVT implementation is higher than that of the SVT implementation.

Low threshold voltages offer the highest circuit performance available in each technology at the cost of increased leakage current. There are two main components of IC leakage current. The dominant leakage current component is the leakage from drain to source of the device which is exacerbated in the LVT devices. LVT field effect transistors (FETs) turn on faster than standard SVT FET devices, but never really turn off fully when the gate voltage is below threshold allowing the leakage current to pass from the drain to source. The second leakage current component is gate tunneling leakage current caused by the thin oxide of the device gate. A thin oxide on the gate does not completely insulate the device and allows leakage current to pass through the gate.

Several techniques have been used to address the leakage problem such as using only high performance LVT circuits in the critical path and using the slower circuits with less leakage elsewhere on the chip. Circuit libraries are available in several variations of VTs which can be mixed and matched throughout the chip. Very complex chip methodologies are used to determine where a LVT circuit should be used in place of a Standard VT (SVT) circuit to increase performance. There are hard limits on the number of LVT circuits used on a chip to keep the leakage current under control. The goal is to get the highest performing circuits paths without violating leakage current limits. Using this technique a chip would be laid out using circuits from the SVT library. A timing run would be performed to determining the critical path circuits. Circuits in the critical path would be replaced with the logically equivalent circuits from the LVT library until the maximum number of LVT circuits is used to meet the leakage power requirement. This iterative process can consume many hour of CPU time performing chip layout, RC extraction and timing analysis before a final design is complete.

A need exists for a mechanism for implementing application specific integrated circuit (ASIC) designs having high performance and reduced leakage current.

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Summary of the Invention

Important aspects of the present invention are to provide a method, circuit library and computer program product for implementing application specific integrated circuit (ASIC) designs having enhanced performance and

5 reduced leakage current. Other important aspects of the present invention are to provide such method, circuit library and computer program product for implementing application specific integrated circuit (ASIC) designs having enhanced performance and reduced leakage current substantially without negative effect and that overcome some of the disadvantages of prior art

10 arrangements.

In brief, a method, apparatus and computer program product are provided for implementing application specific integrated circuit (ASIC) designs having enhanced performance and reduced leakage current. Standard voltage threshold (SVT) circuits in a SVT circuit library are

15 identified. For each SVT circuit, each SVT PFET is replaced with a low voltage threshold (LVT) PFET to provide a hybrid alternate voltage threshold (AVT) circuit. Then the AVT circuits are saved in an alternate voltage threshold circuit library.

In accordance with features of the invention, the alternate voltage

20 threshold circuit library provides enhanced performance as compared to the SVT circuit library without the high leakage current resulting from a LVT circuit library. For every circuit in the SVT library a single shape or low voltage threshold mask is added over the Nwell region to convert the SVT PFETs to LTV PFETs. Converting the SVT PFETs to LVT PFETs results in

25 a much faster rise time for any given circuit.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings,

30 wherein:

FIG. 1A and 1B illustrate a conventional SVT inverter circuit;

FIG. 2A and 2B illustrate a conventional LVT inverter circuit;

FIG. 3A and 3B illustrate an alternate voltage threshold (AVT) inverter circuit in accordance with the preferred embodiment;

FIGS. 4 and 5 are block diagram representations illustrating a computer system and operating system for implementing application specific integrated circuit (ASIC) designs having enhanced performance and reduced leakage current in accordance with the preferred embodiment;

FIG. 6 is a flow chart illustrating exemplary steps for implementing application specific integrated circuit (ASIC) designs having enhanced performance and reduced leakage current in accordance with the preferred embodiment; and

FIG. 7 is a block diagram illustrating a computer program product in accordance with the preferred embodiment.

Detailed Description of the Preferred Embodiments

In accordance with features of the preferred embodiment, a method is provided to solve to the leakage problem that implements an alternate circuit library having an alternate voltage threshold (AVT). The AVT library is a compromise library between the conventional SVT library and the conventional LVT library. The AVT library results in enhanced or improved performance over the conventional SVT library and in reduced leakage current than the conventional LVT library with the added cost of only an additional processing mask.

In accordance with features of the preferred embodiment, the AVT circuit library has been designed that has higher performance as compared to the SVT circuit library without the high leakage of the LVT circuit library. The improved results in performance and leakage current parameters are achieved using the AVT circuit library without the added cost of the AVT mask for processing.

In accordance with features of the invention, all the PFETs in the SVT circuit library are replaced with LVT PFETs. Due to the nature of PFETs, PFETs are larger and slower than NFETs in any given CMOS technology. Converting the SVT PFETs to LVT PFETs results in a much faster rise time for any given circuit. The SVT NFET controls the leakage current to ground when the NFET is in the off state. Assuming an even distribution of "1" and "0" states on a chip, the SVT NFET keeps the leakage current to one-half the leakage current that an equivalent LTV circuit would allow. The fall time of the SVT NFET remains the same, but the circuit is more balanced because the faster rise time of the LVT PFETs more closely matches the fall time of SVT NFET's.

Referring now to the drawings, in FIGS. 3A and 3B, there is shown an exemplary inverter circuit generally designated by the reference character 300 implemented in accordance with a method of the preferred embodiment. FIG. 3A shows a schematic of the new inverter circuit 300 stored in a standard cell AVT library, and FIG. 3B show the corresponding layout of the new inverter circuit 300 of the invention. The inverter circuit 300 is used to demonstrate an exemplary implementation of the method and the AVT circuit of the AVT circuit library of the invention. It should be understood that the present invention is not limited to the illustrated inverter circuit 300, each circuit in a SVT circuit library is processed and stored in the AVT circuit library of the invention.

The inverter circuit 300 includes a series connected P-channel field effect transistor (PFET) 302 and an N-channel field effect transistor (NFET) 304, each having an gate receiving an input A and providing an inverted output labeled Z at a common drain connection.

In accordance with features of the invention, the PFET 302 is a LVT device and the NFET 304 is a SVT device. As shown in FIG. 3B, a low voltage threshold mask or LVT shape is added only over the Nwell Region to convert a SVT PFET to the LTV PFET 302. The PFET 302 is isolated from the NFET 304 and the NFET 304 is maintained as a SVT NFET.

In accordance with features of the invention, implementation of the AVT circuit library of the invention is very simple due to the nature of

standard cell or gate array layouts. All the PFETs in the Nwell Region are isolated from the NFETs. For every circuit in the SVT library, a single shape or low voltage threshold mask is added over the Nwell region to convert the SVT PFETs to LTV PFETs. Once an SVT library is designed, an entire

5 hybrid AVT library can be post-processed in minutes.

Referring now to the drawings, in FIGS. 4 and 5 there is shown a computer system generally designated by the reference character 400 for implementing enhanced performance with reduced leakage current for ASIC designs in accordance with the preferred embodiment. Computer system

10 400 includes a main processor 402 or central processor unit (CPU) 402 coupled by a system bus 406 to a memory management unit (MMU) 408 and system memory including a dynamic random access memory (DRAM) 410, a nonvolatile random access memory (NVRAM) 412, and a flash memory 414. A mass storage interface 416 coupled to the system bus 406 and MMU 408

15 connects a direct access storage device (DASD) 418 and a CD-ROM drive 420 to the main processor 402. Computer system 400 includes a display interface 422 coupled to the system bus 406 and connected to a display 424.

Computer system 400 is shown in simplified form sufficient for

20 understanding the present invention. The illustrated computer system 400 is not intended to imply architectural or functional limitations. The present invention can be used with various hardware implementations and systems and various other internal hardware devices, for example, multiple main processors.

25 As shown in FIG. 5, computer system 400 includes an operating system 430, an electronic package design program 432, a LVT PFET design program 434 of the preferred embodiment, and a user interface 436.

Referring now to FIG. 6, there are shown exemplary steps for implementing enhanced performance with reduced leakage current for ASIC

30 designs in accordance with the preferred embodiment. Standard voltage threshold (SVT) circuits in a SVT circuit library are identified as indicated in a block 600. For each SVT circuit, an LVT votage threshold mask is added over the Nwell region to convert all SVT PFETs low voltage threshold (LVT)

PFETs to provide a hybrid alternate voltage threshold (AVT) circuit as indicated in a block 602. Then the AVT circuits are saved in an alternate voltage threshold (AVT) circuit library as indicated in a block 604.

5   Referring now to FIG. 7, an article of manufacture or a computer program product 700 of the invention is illustrated. The computer program product 700 includes a recording medium 702, such as, a floppy disk, a high capacity read only memory in the form of an optically read compact disk or CD-ROM, a tape, a transmission type media such as a digital or analog communications link, or a similar computer program product. Recording

10   medium 702 stores program means 704, 706, 708, 710 on the medium 702 for carrying out the methods for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs of the preferred embodiment in the system 400 of FIG. 4.

    A sequence of program instructions or a logical assembly of one or

15   more interrelated modules defined by the recorded program means 704, 706, 708, 710, direct the computer system 400 for implementing enhanced performance and reduced leakage current for application specific integrated circuit (ASIC) designs of the preferred embodiment.

    While the present invention has been described with reference to the

20   details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.

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